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PATENT APPLICATION

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IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): James J. deBlanc; et al.

Confirmation No.: 3268

Application No.: 09/872,924

Examiner: LEE, Christopher

Filing Date: June 1, 2001

Group Art Unit: 2112

Title: FAULT TOLERANT BUS FOR HIGHLY AVAILABLE STORAGE ENCLOSURE

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on **August 13, 2004**.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $340.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

(✘) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

(✘)	one month	$110.00	**extension of time fee paid by separate enclosed check**
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( )	four months	$1530.00	

( ) The extension fee has already been filled in this application.

( ) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of **$340.00**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Respectfully submitted,

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Date: **Nov 10, 2004**

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10007686-1 Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of:

James J. deBlanc

Application No: 09/872,924

Filed: June 1, 2001

For: FAULT TOLERANT BUS WITH HIGHLY AVAILABLE STORAGE ENCLOSURE

Examiner: LEE, Christopher

Art Unit: 2112

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November 10, 2004
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William D. Davis

Appeal Brief Under 37 C.F.R. § 41.37

Applicant (Appellant) respectfully submits this brief in support of an appeal from the Examiner's Final Office Action dated April 13, 2004 that finally rejected claims 4, 9, 10, 12-18, and 20. Appellant respectfully requests consideration of this Appeal by the Board of Patent Appeals and Interferences for allowance of the above-referenced application.

The Brief is nominally required to be filed within two months from the date of receipt of the Notice of Appeal (MPEP § 512). The Office stamped a receipt date of August 17, 2004 on Appellant's return postcard thus establishing a due date of October 17, 2004. Accompanying this Brief is a Petition for Extension of Time and fee sufficient for a one month extension of time ending November 17, 2004. Appellant respectfully submits that this Brief is submitted on or before November 17, 2004 as indicated by the above certificate of mailing and thus this Brief is timely filed in accordance with 37 C.F.R. § 41.37 and § 1.136.

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I. REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company, LP, a limited partnership established under the laws of the State of Texas and having a principal place of business at 20555 S.H. 249 Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

II. RELATED APPEALS AND INTERFERENCES

Appellant is unaware of any other related appeals or interferences that may directly affect or be directly affected by or have a bearing on the Board's decision in this pending appeal.

III. STATUS OF THE CLAIMS

Claims 1-5, 7, 9-18, and 20 are pending. Claims 1-3, 5, 7, and 11 are allowed. Claims 4, 9, 10, 12-18, and 20 are rejected. In particular, claim 10 was rejected under 35 U.S.C. § 112, first paragraph. Claims 4 and 9 were rejected under 35 U.S.C. § 112, second paragraph. Claims 12, 13, 14, 15, 16, 17, 18, and 20 were rejected under 35 U.S.C. § 103 as being unpatentable over various combinations of U.S. Patent No. 5,568,063 of Takekuma ("Takekuma"), U.S. Patent No. 5,382,841 of Feldbaumer ("Feldbaumer"), U.S. Patent No. 6,297,663 of Matsuoka, et al. ("Matsuoka"), U.S. Patent No. 4,445,048 of Graham ("Graham"), U.S. Patent No. 5,564,024 of Pemberton ("Pemberton"), U.S. Patent No. 6,011,710 of Wiggers ("Wiggers"), and U.S. Patent No. 5,572,685 of Fisher ("Fisher"). Appellant is appealing the rejection of all of claims 4, 9, 10, 12-18, and 20.

IV. STATUS OF AMENDMENTS

An amendment was submitted on August 13, 2004 subsequent to the final Office Action. The submission made no claim amendments. The

Advisory Action mailed on August 3, 2004 indicates that the amendment after final was not entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

A. Overview

A fault tolerant bus includes signal lines shared among a plurality of electronic devices. The fault tolerant bus is designed to permit failure of one or more attached electronic devices without inhibiting the ability of the bus to change states. (Specification, p. 2).

B. Summary of Claim 1

Claim 1 is allowed, however, an analysis of claim 1 is required with respect to the rejections made against dependent claims 9 and 10.

Claim 1 is drawn to a backplane apparatus including a common bus with a plurality of signal lines. Referring to one embodiment illustrated in Figure 1, each signal line (100) of the common bus has a current limiting element (RA) of impedance RA d.c. coupled to a first supply level (VCC). The apparatus includes isolation circuitry (RD) for electrically coupling each of the plurality of signal lines of the common bus to a corresponding plurality of signal lines of an electronic device (110) to enable communication between the common bus and the electronic device through the isolation circuitry. The isolation circuitry has an impedance RD, wherein (RA+RD) $\geq$3.3 KΩ, wherein RD $\leq$ 25 KΩ. (Specification, p. 6, line 9 through p. 8, line 7; Figure 1)

C. Summary of Claim 4

Claim 4 depends from allowed claim 1 which requires (RA+RD) $\geq$3.3 KΩ and RD $\leq$ 25 KΩ. Claim 4 imposes an additional limitation on the lower bound of RD. In particular, claim 4 requires RD to have a value in a range of approximately 1 KΩ to 25 KΩ. (Specification, p. 7, lines 7-15; p. 8, lines 4-7; p. 10, lines 22-26)

D. Summary of Claim 9

Claim 9 depends from allowed claim 1. Claim 9 imposes an additional limitation on the isolation circuitry. In particular, claim 9 requires the isolation circuitry to comprise (i.e., include) passive components. (Specification, p. 11, lines 17-27; see also, original claim 9)

E. Summary of Claim 10

Claim 10 depends from allowed claim 1. Claim 10 imposes an additional limitation on the isolation circuitry. In particular, claim 10 requires the isolation circuitry to comprise (i.e., include) active components. (Specification, p. 11, lines 17-27; see also, original claim 10)

F. Summary of Claim 12

Claim 12 is drawn to a common bus with a plurality of signal lines. Referring to Figure 1, each signal line of the common bus (100) has a current limiting element (RA) of impedance RA d.c. coupled to a first supply level (VCC). The apparatus includes isolation circuitry (RD) electrically coupling each of the plurality of signal lines of the common bus to a plurality of electronic devices (110). Each device has a corresponding plurality of signal lines to enable communication between the common bus and the plurality of electronic devices. Each signal line of the common bus has associated switching circuitry (140). Each switching circuitry selectively couples a second terminal of its associated first current limiting element (i.e., RA) to a second supply level (embodied as signal ground) to select a logic level of the associated signal line. (Specification, p. 6, line 9 through pg. 7, line 7; Fig. 1).

VI. GROUNDS OF REJECTION TO BE REVIEWED UPON APPEAL

The rejection of claim 10 under 35 U.S.C. § 112, first paragraph is presented for review.

The rejection of claim 4 under 35 U.S.C. § 112, second paragraph is presented for review.

The rejection of claim 9 under 35 U.S.C. § 112, second paragraph is presented for review.

The rejection of claims 12-18 and 20 under 35 U.S.C. § 103 is presented for review.

VII. ARGUMENT

A. Rejection of claim 10 under 35 U.S.C. § 112, first paragraph

Claim 10 was rejected under 35 U.S.C. § 112, first paragraph. The Examiner stated that the specification was "enabling for achieving sufficient isolation by active circuitry instead of passive components" but

> does not reasonably provide enablement for achieving sufficient isolation by passive components (i.e., RD) *and* active circuitry (i.e., together...) The Examiner doubts why the claimed invention needs 'passive components' and 'active circuitry' for achieving sufficient isolation because the specification states 'alternatively, active circuitry such as transistors and operational amplifiers may be used instead of passive components to achieve isolation...'

(04/13/2004 Final Office Action, p. 2)(*emphasis added*)

Appellant notes that the isolation circuitry of claim 1 is not limited explicitly or implicitly to either passive or active components.

Appellant respectfully submits that the Examiner's argument is based on an improper interpretation of claim 1. In particular, the Examiner is improperly limiting the isolation circuitry of claim 1 to the single embodiment consisting of a single inline resistor. This legal error forms the basis for the Examiner's rejection of claims 4, 9, and 10. Thus Appellant must first address whether allowed claim 1 is limited to isolation circuitry consisting of a single inline resistor (RD) passive component.

1) Impedance RD of claim 1 not inherently limited to an inline resistor

In view of the comments the Examiner has made with respect to claims 1, 9, and 10, appellant submits that the Examiner has improperly limited the scope of the terms "impedance" and "RD" from allowed claim 1.

In a subsequent portion of the Final Office Action, the Examiner has misquoted or at least taken out of context a portion of the specification in support of his argument. In particular, the Examiner has stated:

> In fact, the Applicants define RD as an inline resistor (See Application, page 2, lines 20-22). However, the Applicants recite the broader limitation "the isolation circuitry comprises passive components" in the claim 9 since the subject matter "passive components" could be interpreted as an LC circuitry in addition to the resistor circuitry.

(04/13/2004 Final Office Action, p. 3)

In the Advisory Action, the Examiner stated:

> In res[p]onse to the Applicants' arguments regarding to Claim 10 rejection under 35 U.S.C. § 112, first paragraph on the Response pages 6-8, the Examiner respectfully disagrees.
> In fact, the claimed subject matter "RD" is clearly defined in the specification, as an inline resistor (See Application, page 2, lines 20-22). Therefore, the claimed subject matter "impedance RD" should be interpreted as an impedance of the inline resistor (i.e., passive component).

(08/03/2004 Advisory Action, p. 2)

Appellant traverses the Examiner's characterization of appellant's own specification and claim 1. *The language of claim 1 does not limit the claimed isolation circuitry to passive or active circuitry. In particular, the language of claim 1 does not limit the claimed isolation circuitry to a passive component comprising a single inline resistor of value RD.*

The Examiner is obligated to give claims their broadest reasonable interpretation consistent with the specification (In re Hyatt, 54 USPQ2d 1664, 1667; 211 F.3d 1367, 1372 (Fed. Cir. 2000), see also In re American Academy of Science Tech Center, 70 USPQ2d 1827, 1830; 367 F.3d 1359, 1364 (Fed. Cir. 2004). *Even if the appellant had disclosed only a single embodiment, the Examiner is not permitted to limit construction of the claim to the single embodiment.* (Liebel-Flarsheim Co. v. Medrad Inc., 69 USPQ2d 1801, 1807; 358 F.3d 898, 906 (Fed. Cir. 2004); see also, Altiris Inc. v. Symantec Corporation, 65 USPQ2d 1865, 1869-1870; 318 F.3d 1363, 1371 (Fed. Cir. 2003)).

In the present case, despite the specification, claim language, presence of dependent claims, and appellant's prior arguments, the Examiner is continuing to improperly impose limitations in claim 1.

Appellant notes that the limitations that the Examiner is attempting to impose on claim 1 are not explicitly present in the claim, nor is such a limitation implicitly required. As discussed below, the appellant has provided

explicit language in the specification to pre-emptively avoid the Examiner's interpretation. Appellant notes that another illustrated embodiment (Figure 4) contemplates isolation circuitry having a pull-up resistor in addition to an inline resistor. Finally, appellant notes the presence of original proper dependent claims 9 and 10 that should further ensure that claim 1 (in accordance with the doctrine of claim differentiation) is not so narrowly construed.

The Board is referred to the very portion of the specification cited by the Examiner along with the surrounding text as follows:

> The backplane further includes isolation circuitry for electrically coupling each of the plurality of signal lines of the common bus to an electronic device through the isolation circuitry. In one embodiment, the electronic device is removably attached to the backplane signal lines through a connector. *In one embodiment, the isolation circuitry includes an inline resistor, RD, coupling at least one signal line from the common bus to the electronic device.* The isolation circuitry association with some signal lines may further comprise pull up resistors.

(Specification, p. 2, lines 16-23)(*emphasis added*)

Appellant notes that this is the "Summary" which inherently omits details and all the variations discussed in the remainder of the specification. Nonetheless, *even the Summary* clearly states "*in one embodiment*" which hardly supports the Examiner's position that the only embodiment possible for RD is a passive component resistor.

With respect to the figures, the specification states:

> *The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like references indicate similar elements and in which:*
>
> Figure 1 illustrates *one embodiment* of a method of isolating individual drive signal lines sufficiently from a common bus to prevent electrical failure of a single device from substantially interfering with communications on the common bus to the remaining drives.
>
> ...
>
> Figure 4 illustrates *one embodiment* of a method of isolating individual drive signal lines with pull up resistors sufficiently from a common bus to prevent electrical failure of a single device from substantially interfering with communications on the common bus to the remaining drives.

(Specification, p. 3, lines 5-20)(*emphasis added*)

The text discussing Figure 1 states in part:

> *In this embodiment* a single isolation resistor RD, couples each drive to a stub coupled to the common bussed signal.

(Specification, p. 6, lines 12-13)(*emphasis added*)

Figure 4 illustrates isolation circuitry including a resistor RD with a pull-up resistor, 426. Thus at least one other embodiment of isolation circuitry is illustrated. The text discussing Figure 4 states in part:

> Figure 4 illustrates *one embodiment* of a method of isolating individual drive signal lines with pull up resistors sufficiently from a common bus to prevent electrical failure of a single device from substantially interfering with communications on the common bus to the remaining drives.

(Specification, p. 9, lines 9-12)(*emphasis added*)

The specification also introduces the use of active circuitry for the isolation circuitry:

> Alternatively, active circuitry such as transistors and operational amplifiers may be used instead of passive components to achieve sufficient isolation.

(Specification, p. 11, lines 25-27)

The specification also states:

> In the preceding detailed description, the invention is described with reference to specific exemplary embodiments thereof. Various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the claims. *The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.*

(Specification, p. 11, line 28 through p. 12, line 2)(*emphasis added*)

From the doctrine of claim differentiation, different claims are presumed to be of different scope. As stated previously, claims 9 and 10, still depending from claim 1 in their original form, alternatively claim that the isolation circuitry includes passive components (claim 9) or active components (claim 10). Accordingly, the doctrine of claim differentiation also implies that claim 1 is not limited to passive components or active components, much less the very narrow limitation that the Examiner keeps asserting.

Appellant submits 1) the continued usage of the phrases "in one embodiment", "in this embodiment" in the specification and the description

of the figures, 2) the alternative embodiments of isolation circuitry discussed in the specification and illustrated in the figures, and 3) the inferential treatment afforded to claim 1 by the doctrine of claim differentiation with respect to claims 9 and 10 - all bolster appellant's position rather than the Examiner's position with respect to claim 1.

In summary, the isolation circuitry of claim 1 is neither explicitly nor implicitly limited to a "single inline resistor", nor is the isolation circuitry explicitly or implicitly limited to passive components or active components.

2) Claim 10 patentable with proper interpretation of claim 1

The rejection of claim 10 is the result of an improper limitation imposed by the Examiner on claim 1. Appellant respectfully submits that the specification is sufficiently enabling to support active or passive isolation circuitry that maintains the claimed impedance RD such that (RA+RD) $\geq$3.3 KΩ and RD $\leq$25 KΩ. In particular, appellant respectfully submits that there is sufficient enablement for the language of claim 1 as follows:

> 1. A backplane apparatus comprising:
> a common bus comprising a plurality of signal lines, each signal line of the common bus having a current limiting element of impedance RA d.c. coupled to a first supply level; and
> *isolation circuitry* for electrically coupling each of the plurality of signal lines of the common bus to a corresponding plurality of signal lines of an electronic device to enable communication between the common bus and the electronic device through the isolation circuitry, *the isolation circuitry having an impedance RD*, wherein (RA+RD)$\geq$3.3KΩ, wherein RD$\leq$25KΩ.

(Claim 1)(*emphasis added*)

Claim 1 in fact has been allowed. Any claim that further limits claim 1 is a proper dependent claim. As noted above, claim 1 does not include any characterization as to whether the isolation circuitry includes active components. Claim 10 imposes the additional limitation that the isolation circuitry includes active components as follows:

> 10. The apparatus of claim 1 wherein *the isolation circuitry comprises active components.*

(Claim 10)(*emphasis added*)

The Examiner has already acknowledged support for the use of isolation circuitry comprising active components (4/13/2004 Final Office Action, p. 2 citing Specification, p. 11, lines 20-27). Accordingly there should be no remaining impediment to the allowability of claim 10.

Thus appellant respectfully submits claim 10 is enabled in accordance with 35 U.S.C. § 112, first paragraph. Appellant respectfully submits that the 35 U.S.C. § 112, first paragraph rejection of claim 10 is based solely on an improper interpretation of claim 1 and that the rejection otherwise has no merit. Appellant respectfully submits that the Board should find claim 10 allowable.

B. Rejection of claim 4 under 35 U.S.C. § 112, second paragraph

Claim 4 was rejected under 35 U.S.C. § 112, second paragraph. With respect to claim 4, the Examiner has indicated that the term "approximately" renders the claim indefinite because no one could define the values of "approximately 1 KΩ to 25 KΩ".

1) Dependent claim setting forth range narrower than that of its independent claim is not improper under 35 U.S.C. § 112, second paragraph

MPEP 2173.05(c) notes that "it is not improper under 35 U.S.C. § 112, second paragraph to present a dependent claim that sets forth a narrower range for an element than the range set forth in the claim from which it depends."

Appellant notes that claim 4 is a *dependent* claim from an already allowed claim (claim 1). Claim 4 imposes *additional limitations* on the range of values for RD *such that the range expressed in claim 4 is necessarily a subset of the range permitted by claim 1.*

Appellant respectfully submits that in view of a) the range constraints of RD already defined in allowed claim 1, and b) the language of claim 4 that defines the range of RD as a subset of the range defined in allowed claim 1, the range of claim 4 should not be rejected under 35 U.S.C. § 112, second paragraph for indefiniteness (see MPEP 2173.05(c) part I).

2) *"Approximately" permits clear warning that exactitude not required*

Appellant respectfully submits that the use of "approximately" is commonplace with respect to defining ranges. "Approximately" is similar in meaning to "about" or "near". The meaning of the word "about" (and by analogy, "approximately") is dependent upon the facts of the case, the nature of the invention, and the knowledge imparted by the totality of the disclosure to those skilled in the art (Eiselstein v. Frank, 34 USPQ2d 1467, 1471; 52 F.3d 1035, (Fed. Cir. 1995).

The specification states:

> Clearly the values selected for RD and RA depend upon a number of factors including the specified operational constraints, VCC, and whether a pullup resistor is used.

(Specification, p. 10, lines 22-24)

The values selected are also dependent upon the number of drives for which failure isolation is desired. Equations describing RD evaluated with assumed operating constraints are set forth at Specification, pp. 6-8 (without pull-up resistor). The specification also notes a tolerance for resistors recognizing a difference in nominal and actual resistance values. With the number of variables affecting the computation of RD, appellant respectfully submits that claim 4 makes fair use of the term "approximately". Moreover, the claim language is explicitly supported at Specification, p. 10, line 24-26.

Appellant submits that given the nature of the invention (failure isolation for an integer number of drives), the facts of the case (e.g., the particular operational constraints, choice of VCC and RA, whether a pullup resistor is used, etc.), and the knowledge imparted by the totality of the disclosure to those skilled in the art (e.g., the complex relationship between RA, RD, VCC, desired drive immunity, and operational constraints), *the specification provides sufficient reference for the meaning of "approximately" to one skilled in the art.*

Appellant respectfully submits that the rejection of claim 4 under 35 U.S.C. § 112, second paragraph was improper. Appellant respectfully submits that the Board should find claim 4 allowable.

C. Rejection of claim 9 under 35 U.S.C. § 112, second paragraph

The Examiner has rejected claim 9 under 35 U.S.C. § 112, second paragraph as being indefinite because of the language that "the isolation circuitry comprises passive components" which the Examiner believes is broader than the limitation of the parent claim of "the isolation circuitry having an impedance RD". (04/13/2004 Office Action, p. 3)

Appellant notes that the language of claim 1 does not explicitly state nor does it imply that the impedance RD is embodied as active or passive components. Indeed the existence of dependent claims 9 (passive components) and 10 (active components) should ensure that claim 1 is not limited particularly to either passive or active circuitry by the doctrine of claim differentiation as previously discussed.

As was the case with the rejection of claim 10 above, the Examiner has impermissibly added non-existent limitations to re-define the scope of appellant's claim 1. The Examiner is obligated to give claims their broadest reasonable interpretation consistent with the specification (see, e.g., In re Hyatt, 54 USPQ2d 1664, 1667; 211 F.3d 1367, 1372 (Fed. Cir. 2000). In the present case, despite the specification, claim language, presence of dependent claims, and appellant's prior arguments, the Examiner is continuing to improperly impose limitations that do not appear in claim 1.

Appellant has presented these arguments in greater detail with respect to the rejection of claim 10 above. If the Board agrees that the impedance RD of claim 1 is not limited to an inline resistor, then there is no basis for the rejection of either claim 9 or 10.

Appellant agrees that "passive components" can include components other than resistors. (see 04/13/2004 Office Action, p. 3) Contrary to the Examiner's interpretation, however, parent claim 1 does not limit the isolation circuitry to passive or active circuitry.

Claim 9 includes the language:

> 9. The apparatus of claim 1 *wherein the isolation circuitry comprises passive components.*

(Claim 9)(*emphasis added*)

Claim 9 thus adds the limitation that the isolation circuitry includes passive components. Claim 9 is a proper dependent claim because it adds further structure and limitations to claim 1. The passive component limitation of claim 9 necessarily narrows claim 1 because claim 1 did not impose any such restrictions on the isolation circuitry. The isolation circuitry of claim 1 is neither explicitly nor implicitly limited to active or passive components nor did it exclude active components, passive components, or combinations of active and passive components.

Given that claim 9 was apparently rejected based on a non-existent limitation improperly imposed by the Examiner with respect to claim 1, appellant respectfully submits that the rejection of claim 9 under 35 U.S.C. § 112, second paragraph was improper. Appellant respectfully submits that the Board should find claim 9 allowable.

D. Rejection of claims 12-18 and 20 under 35 U.S.C. § 103

Claims 12-18 and 20 were rejected under 35 U.S.C. § 103 over Takekuma, Feldbaumer, and Matsuoka with various combinations of Graham, Pemberton, Wiggers, and Fisher. Appellant will address these rejections as applied to independent claim 12.

In order to sustain a rejection under 35 U.S.C. § 103, three criteria must be met:

> *First*, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. *Second*, there must be a reasonable expectation of success. *Finally*, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure

(*In re Vaeck*, 20 USPQ2d 1438; 947 F.2d 488 (Fed. Cir. 1991)(*emphasis added*)

Appellant respectfully submits that the Examiner has failed to establish even a *prima facie* case of obviousness under 35 U.S.C. § 103 and therefore claims 12-18 and 20 were improperly rejected under 35 U.S.C. § 103 in view of the cited references.

1) Characterization of references

Appellant need only address the references cited in rejecting claim 12. However, appellant believes that a characterization of the various references cited may be pertinent.

Takekuma includes a disclosure of a bus or "inter-block" transmission line having a plurality of elements including a driving element and a plurality of receivers coupled to it. Each element includes an "intra-block" for communicating between the receiver or driver as the case may be to the inter-block transmission line. The inter-block transmission line is terminated at both ends by resistors coupled to a power supply (1.5 volts). The intra-block transmission lines are coupled through a resistor to the inter-block transmission line. The value of the resistors coupling the intra-blocks to the inter-block is set to the impedance of the intra-block transmission line minus 1/2 the impedance of the inter-block transmission line. (Takekuma, col. 4, lines 44-67; Fig. 4, 11, 14, 15, 20, 21, 27)

Feldbaumer includes a disclosure of a switchable active bus termination circuit within a peripheral device for coupling/decoupling a terminating resistor to a voltage reference source. The switchable terminating resistor eliminates the requirement of manually inserting a single in-line package (SIP) containing a terminating resistor array for the last peripheral device on a SCSI bus or removing such a SIP when the peripheral is not the last device on the bus (Feldbaumer, col. 1, lines 53-64; col. 2, lines 3-18; col. 4, lines 19-22; Figs. 1, 2)

Matsuoka includes a disclosure of a bus having a plurality of terminated signal lines to support communication between first and second memory buffers and a memory controller. A first set of series resistors is provided within the signal lines between the first memory buffer and the controller. A second set of series resistors is provided within the signal lines between the second memory buffer and the controller (Matsuoka, col. 2, line 60 - col. 3, line 23; Figs. 1, 2A)

Graham includes a disclosure of a high speed ribbon cable bus for connecting a plurality (n) of units. Each unit includes one driver and a plurality (at least n-1) of receivers. Receivers are coupled to conductor pairs of

the ribbon cable through resistors using connectors that have spaced apart pins to reduce capacitive coupling between conductors. (Graham, col. 2, lines 5-39; Figs. 1-2).

Pemberton includes a disclosure of an active termination circuit at the end of a SCSI bus to protect devices on a SCSI peripheral device chain during addition or removal of a SCSI device from an active (powered) bus. Pemberton teaches a removal sequence including: asserting a reset signal of the powered bus; disconnecting all signal lines of the peripheral device from the bus; and then de-asserting the reset signal. The peripheral device may then be removed without removing power from the bus. To add a device, Pemberton teaches the sequence including: asserting a reset signal of the powered bus; connecting the logic ground and then the other signal lines of the peripheral device to the bus; and then de-asserting the reset signal. Initiating the sequence requires toggling a switch on an active termination circuit that is at the end of the device chain (Pemberton, col. 3, lines 15-59; col. 6, lines 8-49; Figs. 3-4)

Wiggers includes a disclosure of a memory having a bus with reduced capacitive load for communication between memory devices and a controller. Rather than leaving all the memory devices coupled to the same bus, Wiggers provides switching circuitry to couple each individual memory device to the bus only when access to a memory location within that device is required. (Wiggers, col. 3, lines 16-67; Figs. 4, 6)

Fisher discloses a backplane for coupling a host processor to a plurality of disk drive units. The backplane includes isolation circuitry comprising a set of bus switches to isolate all the devices on the bus from an initiator device and a target device so as to reduce bus capacitance and reflections. (Fisher, col. 1, lines 28-56; Fig. 1).

2) ***References alone or combined do not teach or suggest all claim limitations***

Matsuoka has been cited merely for extending the combination of Feldbaumer and Takekuma from one signal line to a plurality of signal lines. Takekuma is relied upon by the Examiner for a number of elements,

particularly the first current limiting element d.c. coupled to a first supply level and the isolation circuitry. The Examiner notes that Takekuma does not disclose and has relied upon Feldbaumer for disclosing: a switching circuit selectively coupling a second terminal of the associated first current limiting element to a second supply level to select a logic level of the associated signal line. (4/13/2004 Final Office Action, p. 4).

In particular, the Examiner has stated:

> Feldbaumer discloses a switchable active bus termination circuit (Fig. 1), wherein said bus termination circuit comprising switching circuitry (i.e., switching circuit 18 of Fig. 1) for signal line of a common bus (i.e., electrical conductor 21 of Fig. 1), wherein said switching circuitry selectively couples a second terminal (i.e., connection point on terminal resistor 20 for switching circuit 18 in Fig. 1) of an associated first current limiting element (i.e., resistor 20 of Fig. 1) to a second supply level to select a logic level of said associated signal line (See col. 2, lines 54-65).

(4/13/04 Final Office Action, p. 4)

Appellant respectfully traverses the Examiner's characterization of Feldbaumer. Feldbaumer subsequently discloses selectable active termination circuitry for incorporation into a peripheral device so that manual insertion/removal of a resistor single in-line package (SIP) can be avoided. In particular, the bus may be terminated through the use of a control signal ($\overline{\text{ENABLE}}$) applied to the active termination circuitry within the last peripheral device on the bus instead of performing a manual insertion or removal of a resistor SIP.

Contrary to the Examiner's assertions, *Feldbaumer's switching circuit 18 is not used to change the logic levels of signal line 21.* Communicating logic signals is independent from termination of the signal line. Indeed, given that only the *last* device is terminated and it is terminated for as long as it is the last device, this begs the question as to how any other device could then change the signal line logic level or what the purpose of element 22 is. *Switching circuit 18 is used to enable or disable active termination of the signal line - not to change the bus logic levels.* (see, Feldbaumer, col. 4, lines 1-22).

When termination is disabled, element 20 has one connection point "floating". When $\overline{\text{ENABLE}}$ is asserted, the previously floating terminal of

element 20 is connected to voltage regulator 12. (Feldbaumer, Fig. 1). After appropriately trimming the trimmable resistors 32, 40, and 46, the signal line 21 may be selectively terminated at approximately a 110Ω impedance using the $\overline{\text{ENABLE}}$ control signal. (Feldbaumer, col. 3, lines 5-16, 44-58, col. 4, lines 1-22)

Feldbaumer fails to disclose a switching circuit selectively coupling a second terminal of the associated first current limiting element to a second supply level to select a logic level of the associated signal line.

In contrast, the specification teaches and claim 12 recites:

> 12. A backplane apparatus comprising:
>
> a common bus comprising a plurality of signal lines, each signal line having first terminal of an associated first current limiting element d.c. coupled to a first supply level, the first current limiting element of impedance RA;
>
> isolation circuitry electrically coupling each of the plurality of signal lines of the common bus to a plurality of electronic devices, each device having a corresponding plurality of signal lines to enable communication of signals between the common bus and the plurality of electronic devices; and
>
> *switching circuitry for each signal line of the common bus, wherein each switching circuitry selectively couples a second terminal of the associated first current limiting element to a second supply level to select a logic level of the associated signal line.*

(Claim 12)(*emphasis added*)

3) Proposed combination is unworkable

Even if one accepted *arguendo* the Examiner's characterizations, appellant respectfully submits that it is not clear how the Examiner has proposed combining Takekuma and Feldbaumer in a workable manner consistent with the teachings of both.

For example, is the Examiner proposing substitution of Feldbaumer's active termination circuitry for one or both of the termination resistors 50, 51 of Takekuma? At best, appellant submits that this might result in selectable active termination of both ends of Takekuma's bus - but enabling termination does not switch the logic levels or convey a logic signal on the bus.

Moreover, it is not clear how the Examiner is coupling a first terminal of Takekuma's/Feldbaumer's current limiting element to a first supply level while using the termination circuitry of Feldbaumer to switch a second

terminal of the current limiting element to a second supply level. *Appellant respectfully requests the Examiner to please illustrate his proposed combination and indicate the source of the elements (e.g., Feldbaumer, Takekuma, etc.).*

Appellant respectfully submits that the Examiner's proposed combination is either unworkable or does not work to achieve the alleged results. Appellant respectfully submits that the combination of Takekuma, Feldbaumer and Matsuoka proposed by the Examiner does not teach or suggest *each signal line having a first terminal of an associated first current limiting device d.c. coupled to a first supply level* and *switching circuitry for each signal line of the common bus, wherein the switching circuitry selectively couples a second terminal of the associated first current limiting element to a second supply level to select a logic level of the associated signal line* with *isolation circuitry electrically coupling each signal line to a plurality of electronic devices.*

In contrast, the specification teaches and claim 12 recites:

> 12. A backplane apparatus comprising:
> a common bus comprising a plurality of signal lines, *each signal line having first terminal of an associated first current limiting element d.c. coupled to a first supply level,* the first current limiting element of impedance RA;
> *isolation circuitry electrically coupling each of the plurality of signal lines of the common bus to a plurality of electronic devices,* each device having a corresponding plurality of signal lines to enable communication of signals between the common bus and the plurality of electronic devices; and
> *switching circuitry for each signal line of the common bus, wherein each switching circuitry selectively couples a second terminal of the associated first current limiting element to a second supply level to select a logic level of the associated signal line.*

(Claim 12)(*emphasis added*)

Appellant respectfully submits that the remaining rejections under 35 U.S.C. § 103 were based on additional combinations with Graham, Pemberton, Wiggers, and Fisher. These remaining rejections were presented only with respect to dependent claims. None of these additional references, however, makes up for the deficiencies of Takekuma and Feldbaumer. In view of the arguments presented above, appellant submits claim 12 is patentable in view of all of the cited references.

Given that claims 13-18 and 20 depend from claim 12, appellant respectfully submits claims 13-18 and 20 are likewise patentable under 35 U.S.C. § 103 in view of the cited references.

Appellant respectfully submits that the Board should find claims 12-18 and 20 allowable.

X. CONCLUSION

Appellant respectfully submits that the stated rejections cannot be maintained in view of the arguments set forth above. Claims 4, 9, and 10 are patentable under 35 U.S.C. § 112, first and second paragraphs. With respect to the remaining claims, the references alone or combined do not teach or suggest all the claim limitations. The Examiner has failed to establish even a *prima facie* case of obviousness under 35 U.S.C. § 103. Thus claims 12-18 and 20 are patentable under 35 U.S.C. § 103 in view of the cited references.

Appellant respectfully requests that the Board of Patent Appeals and Interferences direct allowance of the rejected claims 4, 9, 10, 12-18, and 20 such that all of pending claims 1-5, 7, 9-18, and 20 are allowed.

If there are any issues that can be resolved by telephone conference, the undersigned representative of the appellant may be contacted at **(512) 306-9470 or (512) 858-9910.**

Respectfully submitted,

Date: November 10, 2004

William D. Davis
Reg. No. 38,428

CLAIMS APPENDIX

The claims and their amendment status history are presented below.

1. (PREVIOUSLY PRESENTED) A backplane apparatus comprising:

a common bus comprising a plurality of signal lines, each signal line of the common bus having a current limiting element of impedance RA d.c. coupled to a first supply level; and

isolation circuitry for electrically coupling each of the plurality of signal lines of the common bus to a corresponding plurality of signal lines of an electronic device to enable communication between the common bus and the electronic device through the isolation circuitry, the isolation circuitry having an impedance RD, wherein $(RA+RD) \geq 3.3K\Omega$, wherein $RD \leq 25K\Omega$.

2. (ORIGINAL) The apparatus of claim 1 further comprising:

a connector for removably coupling the plurality of signal lines of the electronic device to the plurality of signal lines of the common bus through the isolation circuitry.

3. (PREVIOUSLY PRESENTED) The apparatus of claim 1 wherein the isolation circuitry for each signal line comprises an inline resistor having an impedance of RD.

4. (PREVIOUSLY PRESENTED) The apparatus of claim 1 wherein RD has a value in a range of approximately 1 KΩ to 25 KΩ.

5. (PREVIOUSLY PRESENTED) The apparatus of claim 1 wherein a first terminal of the current limiting element is coupled to the first supply level, wherein the apparatus further comprises switching circuitry, wherein the switching circuitry selectively couples a second terminal of the current limiting element to a second supply level.

6. (CANCELED)

7. (PREVIOUSLY PRESENTED) The apparatus of claim 1 wherein RA is in a range of 10 Ω to 5 KΩ.

8. (CANCELED)

9. (ORIGINAL) The apparatus of claim 1 wherein the isolation circuitry comprises passive components.

10. (ORIGINAL) The apparatus of claim 1 wherein the isolation circuitry comprises active components.

11. (ORIGINAL) The apparatus of claim 1 wherein the electronic device is a disk drive.

12. (PREVIOUSLY PRESENTED) A backplane apparatus comprising:

a common bus comprising a plurality of signal lines, each signal line having first terminal of an associated first current limiting element d.c. coupled to a first supply level, the first current limiting element of impedance RA;

isolation circuitry electrically coupling each of the plurality of signal lines of the common bus to a plurality of electronic devices, each device having a corresponding plurality of signal lines to enable communication of signals between the common bus and the plurality of electronic devices; and

switching circuitry for each signal line of the common bus, wherein each switching circuitry selectively couples a second terminal of the associated first current limiting element to a second supply level to select a logic level of the associated signal line.

13. (ORIGINAL) The apparatus of claim 12 further comprising:

a plurality of connectors for removably coupling the plurality of signal lines of each electronic device to the corresponding plurality of signal lines of the common bus through the isolation circuitry.

14. (PREVIOUSLY PRESENTED) The apparatus of claim 12 wherein the isolation circuitry is passive isolation circuitry.

15. (PREVIOUSLY PRESENTED) The apparatus of claim 14 wherein the isolation circuitry is an inline resistor of impedance RD in a range of 1 KΩ to 25 KΩ.

16. (PREVIOUSLY PRESENTED) The apparatus of claim 14 wherein the isolation circuitry is an inline resistor of impedance RD in conjunction with a pull up resistor, wherein RD is less than 1 KΩ.

17. (PREVIOUSLY PRESENTED) The apparatus of claim 12 wherein the isolation circuitry is active isolation circuitry.

18. (ORIGINAL) The apparatus of claim 12 wherein RA for each selected signal line of the common bus is selected to have a value in a range of 10 Ω to 5 KΩ.

19. (CANCELED)

20. (ORIGINAL) The apparatus of claim 12 wherein the electronic devices include disk drives.

EVIDENCE APPENDIX

No additional evidence has been entered by the Examiner and relied upon by the appellant. Thus this appendix is not applicable.

RELATED PROCEEDINGS APPENDIX

Appellant is unaware of any other related appeals or interferences that may directly affect or be directly affected by or have a bearing on the Board's decision in this pending appeal. Thus this appendix is not applicable.